# Slater & Matsil, L.L.P.

Suite 1000
17950 Preston Road
Dallas, Texas 75252-5793
Phone: 972-732-1001 Facsimile: 972-732-9218


RECEIVED
CENTRAL FAX CENTER
AUG 0 2 2005

## FACSIMILE COVER SHEET

| | | | |
|---|---|---|---|
| To Examiner: | Asok K. Sarkar | Total Pages Sent: | 29 |
| | Technology Center 2800 | (including cover sheet) | |
| Facsimile Number: | (571) 273-8300 | Transmission Date: | August 2, 2005 |

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | | |
|---|---|---|---|
| Applicant: | Low, *et al.* | Docket No.: | 02 P 15173 US / INTECH 3. |
| Serial No.: | 10/689,233 | Art Unit: | 2891 |
| Date Filed: | October 20, 2003 | | |
| TITLE: | Inclusion Of Low-K Dielectric Material Between Bit Lines | | |

## CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to Mail Stop Amendment at the U.S. Patent and Trademark Office at (571) 273-8300 on May 2, 2005:

- Certification of Facsimile Transmission (1 page)
- Amendment (28 pages)

Respectfully submitted,

Kristy Engeldahl

Kristy Engeldahl
Legal Assistant

**Confirmation Respectfully Requested**

This facsimile is intended only for the use of the address named and contains legally privileged and/or confidential information. If you are not the intended recipient of this telecopy, you are hereby notified that any dissemination, distribution, copying or use of this communication is strictly prohibited. Applicable privileges are not waived by virtue of the document having been transmitted by Facsimile. Any misdirected facsimiles should be returned to the sender by mail at the address indicated on this cover sheet.

RECEIVED
CENTRAL FAX CENTER
AUG 02 2005

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | | |
|---|---|---|---|
| Applicant: | Low, *et al.* | Docket No.: | 02 P 15173 US / INTECH 3. |
| Serial No.: | 10/689,233 | Art Unit: | 2891 |
| Filed: | October 20, 2003 | Examiner: | Asok K. Sarkar |
| For: | Inclusion Of Low-K Dielectric Material Between Bit Lines | | |

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

## AMENDMENT

Dear Sir:

The following amendments and remarks are presented in response to the Examiner's Office Action mailed May 2, 2005. Please amend the above-referenced application as follows.



PAGE 2/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

In the Claims:

1. (Currently Amended) A method of incorporating a first dielectric material into a semiconductor device, said semiconductor device being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said semiconductor device at least through [[up to ]]the thermal processing step using a second ~~further~~ dielectric material having a maximum withstand temperature greater than the temperature of the thermal processing step, said second dielectric material formed atop, an etch stop layer, and disposed adjacent at least one conductive line of said semiconductor device;

removing at least a portion of said second ~~further~~ dielectric material down to said etch stop layer; and

depositing a layer of said first ~~lower withstand temperature~~ dielectric material in place of the removed portion of said second ~~further~~ dielectric material.

2. (Currently Amended) The method of claim 1 wherein said first ~~lower withstand temperature~~ dielectric material has a lower dielectric constant than said further dielectric material.

3. (Canceled)



PAGE 3/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

4. (Currently Amended) The method of claim [[3]] 1 wherein said at least one conductive line includes a contact barrier layer, and the thermal processing step is an anneal step of said contact barrier layer.

5. (Canceled)

6. (Canceled)

7. (Currently Amended) The method of claim [[3]] 1 further comprising:

planarizing said first ~~said lower withstand temperature~~ dielectric material to a top surface of said conductive line; and

depositing a further layer of said first ~~lower withstand temperature~~ dielectric material atop said layer of said planarized first ~~said lower withstand temperature~~ dielectric material and atop said conductive line.

8. (Currently Amended) The method of claim [[3]] 1 wherein said step of depositing a layer of said first ~~lower withstand temperature~~ dielectric material includes depositing said layer atop said conductive line; and said method further includes planarizing said layer of said first ~~lower withstand temperature~~ dielectric material such that a portion thereof remains atop said conductive line and serves as an inter-level dielectric layer.

9. (Currently Amended) A method of incorporating a first dielectric material into an insulator structure that is adjacent to at least one conductive line of a semiconductor device, said



PAGE 4/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

insulator structure and said at least one conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said insulator structure and said at least one conductive line at least through [[up to]] the thermal processing step using a second dielectric material that has a maximum withstand temperature greater than the temperature of the thermal processing step, said fabricating step comprising:

depositing a first layer of said second dielectric material atop a surface of a semiconductor substrate,

planarizing said first layer of said dielectric material to a top surface of another conductive line disposed atop said semiconductor substrate,

depositing another layer of said second dielectric material atop said first layer of said second dielectric material and atop said another conductive line,

patterning and etching said another layer of said second dielectric material to form at least one opening therein, and

filling said opening with at least one conducting material to form said at least one conductive line;

removing at least a portion of said second ~~further~~ dielectric material; and

depositing a layer of said first ~~lower withstand temperature~~ dielectric material in place of the removed portion of said second ~~further~~ dielectric material.

10. (Canceled)



PAGE 5/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

11. (Currently Amended) The method of claim 9 wherein said first ~~lower withstand temperature~~ dielectric material has a lower dielectric constant than said second ~~further~~ dielectric material.

12. (Currently Amended) The method of claim 9 wherein said step of fabricating said insulator structure and said conductive line includes: depositing a contact barrier layer prior to depositing said conductive line, and annealing said contact barrier layer at a temperature greater than said maximum withstand temperature of said first ~~lower withstand temperature~~ dielectric material.

13. (Currently Amended) The method of claim 9 wherein an etch stop layer is disposed beneath said second ~~further~~ dielectric material; and wherein said step of removing at least a portion of said second ~~further~~ dielectric material includes etching down to said etch stop layer.

14. (Currently Amended) The method of claim 9 wherein said step of removing at least a portion of said second ~~further~~ dielectric material includes a timed etching step.

15. (Currently Amended) The method of claim 9 further comprising:

planarizing said layer of said first ~~lower withstand temperature~~ dielectric material to a top surface of said conductive line; and

depositing another ~~a further~~ layer of said first ~~lower withstand temperature~~ dielectric material atop said layer of said first ~~another~~ dielectric material and atop said conductive line.



PAGE 6/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

16. (Currently Amended) The method of claim 9 wherein said step of depositing a layer of said first ~~lower withstand temperature~~ dielectric material includes depositing said layer atop said conductive line; and ~~said method includes~~ planarizing said layer of said first ~~lower withstand temperature~~ dielectric material such that a portion thereof remains atop said conductive line and serves as an inter-level dielectric layer.

17. (Withdrawn) A method of fabricating a semiconductor device, said method comprising:

forming at least one deep trench within a semiconductor substrate;

forming a buried plate within a region of said semiconductor substrate that adjoins a bottom of said deep trench;

forming an insulator film along sidewalls of said deep trench;

removing an upper region of said insulator film;

partly filling said deep trench with doped polysilicon that extends above a remaining portion of said insulator film, the dopants in the polysilicon diffusing through at least one side of said deep trench into an adjoining region of said semiconductor substrate during subsequent thermal processing steps to form a buried strap region along said side of said deep trench;

forming a trench top oxide layer atop said doped polysilicon;

forming a gate insulator layer on at least said upper portion of said side of said deep trench;

filling said deep trench with a further polysilicon layer atop said trench top oxide layer;

patterning and etching said semiconductor substrate to form at least one isolation trench that adjoins said deep trench;

filling said isolation trench with an insulator material;



PAGE 7/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

forming a doped region in a top surface of said semiconductor substrate adjacent to said gate insulator layer of said deep trench;

forming a contact region that connects to said further polysilicon layer;

depositing at least one conducting layer atop said contact region to form a first conductive line;

depositing a layer of a first dielectric material atop said surface of said semiconductor substrate;

planarizing said first dielectric layer to said top surface of said first conductive line;

depositing a layer of a further dielectric material atop said first dielectric layer and atop said first conductive line;

patterning and etching said further dielectric layer and said first dielectric layer to form at least one opening therein that includes at least one region that extends down to said doped region adjacent to said gate dielectric;

depositing a contact barrier layer at least at a bottom of said opening;

annealing said contact barrier layer;

filling said opening with at least one further conducting layer to form at least one further conductive line;

removing at least an upper portion of said further dielectric layer to form at least one opening adjacent to said further conductive line; and

depositing a layer of another dielectric material at least in said opening adjacent to said bit line, said another dielectric material having a lower dielectric constant than that of said further dielectric material.



PAGE 8/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

18. (Withdrawn) The method of claim 17 wherein said annealing step is carried out at a temperature greater than a maximum withstand temperature of said another dielectric material.

19. (Withdrawn) The method of claim 17 further comprising: depositing an etch stop layer atop said first dielectric layer prior to depositing said layer of a further dielectric material; and wherein said step of removing at least an upper portion of said further dielectric material includes etching down to said etch stop layer.

20. (Withdrawn) The method of claim 17 wherein said step of removing at least an upper portion of said further dielectric material includes a timed etching step.

21. (Withdrawn) The method of claim 17 further comprising:

planarizing said another dielectric layer to a top surface of said bit line; and

depositing a further layer of said another dielectric material atop said layer of said another dielectric material and atop said further conductive line.

22. (Withdrawn) The method of claim 17 wherein said step of depositing a layer of another dielectric material includes depositing said layer of another dielectric material atop said further conductive line; and said method further comprises planarizing said another dielectric layer such that a portion thereof remains atop said further conductive line and serves as an inter-level dielectric layer.

23. (Withdrawn) A method of fabricating a semiconductor device, said method comprising:



PAGE 9/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

forming a planar gate oxide layer atop a surface of a semiconductor substrate;

depositing at least one conducting layer atop said gate oxide layer;

patterning and etching said at least one conducting layer to form at least two openings therein;

introducing dopants into said substrate through said openings in said at least one conducting layer to form at least one source region and at least one drain region;

depositing a layer of a first dielectric material atop said surface of said semiconductor substrate;

planarizing said first dielectric material to said top surface of said at least one conducting layer line;

depositing a layer of a further dielectric material atop said first dielectric layer and atop said at least one conductive layer;

patterning and etching said further dielectric layer and said first dielectric layer to form at least one opening therein that includes at least one region that extends down to at least one of said source region and said drain region;

depositing a contact barrier layer at least at a bottom of said opening;

annealing said contact barrier layer;

filling said opening with at least one further conducting layer;

removing at least an upper portion of said further dielectric layer to form at least one opening adjacent to said further conducting layer; and

depositing a layer of another dielectric material at least in said opening adjacent to said further conductive layer, said another dielectric material having a lower dielectric constant than that of said further dielectric material.



PAGE 10/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

24. (Withdrawn) The method of claim 23 wherein said annealing step is carried out at a temperature greater than a maximum withstand temperature of said another dielectric material.

25. (Withdrawn) The method of claim 23 further comprising: depositing an etch stop layer atop said first dielectric layer prior to depositing said layer of a further dielectric material; and wherein said step of removing at least an upper portion of said further dielectric material includes etching down to said etch stop layer.

26. (Withdrawn) The method of claim 23 wherein said step of removing at least an upper portion of said further dielectric material includes a timed etching step.

27. (Withdrawn) The method of claim 23 further comprising:

planarizing said another dielectric layer to a top surface of said further conductive layer; and

depositing a further layer of said another dielectric material atop said layer of said another dielectric material and atop said further conducting layer.

28. (Withdrawn) The method of claim 23 wherein said step of depositing a layer of another dielectric material includes depositing said layer of another dielectric material atop said further conducting layer; and said method further comprises planarizing said another dielectric layer such that a portion thereof remains atop said further conducting layer and serves as an inter-level dielectric layer.



PAGE 11/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

29. (Withdrawn) A method of incorporating a dielectric material into an insulator structure of a semiconductor, said insulator structure adjacent to at least one conductive line, said insulator structure and said conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said dielectric material, said process comprising the steps of:

fabricating said insulator structure and said conductive line at least up to the thermal processing step using a further dielectric material that has a maximum withstand temperature greater than the temperature of the thermal processing step;

removing at least a portion of said further dielectric material; and

depositing a layer of said lower withstand temperature dielectric material in place of the removed portion of said further dielectric material.

30. (Withdrawn) The method of claim 29 wherein said fabricating step includes:

depositing a layer of a first dielectric material atop a surface of a semiconductor substrate;

planarizing said first dielectric material to a top surface of an insulated word line disposed atop said semiconductor substrate;

depositing a layer of a further dielectric material atop said first dielectric layer and atop said insulated word line;

patterning and etching said further dielectric material and said first dielectric material to form at least one opening therein; and

filling said opening with at least one conducting material to form at least one bit line.



PAGE 12/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):08-20

31. (Withdrawn) The method of claim 29 wherein said lower withstand temperature dielectric material has a lower dielectric constant than said further dielectric material.

32. (Withdrawn) The method of claim 29 wherein said step of fabricating said insulator structure and said bit line includes: depositing a contact barrier layer prior to depositing said conductive line, and annealing said contact barrier layer at a temperature greater than said maximum withstand temperature of said lower withstand temperature dielectric material.

33. (Withdrawn) The method of claim 29 wherein an etch stop layer is disposed beneath said further dielectric material; and wherein said step of removing at least a portion of said further dielectric material includes etching down to said etch stop layer.

34. (Withdrawn) The method of claim 29 wherein said step of removing at least a portion of said further dielectric material includes a timed etching step.

35. (Withdrawn) The method of claim 29 further comprising:

planarizing said layer of said lower withstand temperature dielectric material to a top surface of said bit line; and

depositing a further layer of said lower withstand temperature dielectric material atop said layer of said another dielectric material and atop said conductive line.

36. (Withdrawn) The method of claim 29 wherein said step of depositing a layer of said lower withstand temperature dielectric material includes depositing said layer atop said



PAGE 13/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

conductive line; and said process includes planarizing layer of said lower withstand temperature dielectric material such that a portion thereof remains atop said conductive line and serves as an inter-level dielectric layer.

37. (Withdrawn) A method of fabricating a semiconductor device comprising the steps of:

forming at least one deep trench within a semiconductor substrate;

forming a buried plate within a region of said semiconductor substrate that adjoins a bottom of said deep trench;

forming an insulator film along sidewalls of said deep trench;

removing an upper region of said insulator film;

partly filling said deep trench with doped polysilicon that extends above a remaining portion of said insulator film, the dopants in the polysilicon diffusing through at least one side of said deep trench into an adjoining region of said semiconductor substrate during subsequent thermal processing steps to form a buried strap region along said side of said deep trench;

forming a trench top oxide layer atop said doped polysilicon;

forming a gate insulator layer on at least said upper portion of said side of said deep trench;

filling said deep trench with a further polysilicon layer atop said trench top oxide layer;

patterning and etching said semiconductor substrate to form at least one isolation trench that adjoins said deep trench;

filling said isolation trench with an insulator material;

forming a doped region in a top surface of said semiconductor substrate adjacent to said gate insulator layer of said deep trench;



PAGE 14/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

forming a contact region that connects to said further polysilicon layer;

depositing at least one conducting layer atop said contact region to form a first conductive line;

depositing a layer of a first dielectric material atop said surface of said semiconductor substrate;

planarizing said first dielectric layer to said top surface of said first conductive line;

depositing a layer of a further dielectric material atop said first dielectric layer and atop said insulated word line;

patterning and etching said further dielectric layer and said first dielectric layer to form at least one opening therein that includes at least one region that extends down to said doped region adjacent to said gate dielectric;

depositing a contact barrier layer at least at a bottom of said opening;

annealing said contact barrier layer;

filling said opening with at least one further conducting layer to form at least one further conductive line;

removing at least an upper portion of said further dielectric layer to form at least one opening adjacent to said bit line; and

depositing a layer of another dielectric material at least in said opening adjacent to said bit line, said another dielectric material having a lower dielectric constant than that of said further dielectric material.

38. (Withdrawn) The method of claim 37 wherein said anncaling step is carried out at a temperature greater than a maximum withstand temperature of said another dielectric material.



PAGE 15/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

39. (Withdrawn) The method of claim 37 further comprising: depositing an etch stop layer atop said first dielectric layer prior to depositing said layer of a further dielectric material; and wherein said step of removing at least an upper portion of said further dielectric material includes etching down to said etch stop layer.

40. (Withdrawn) The method of claim 37 wherein said step of removing at least an upper portion of said further dielectric material includes a timed etching step.

41. (Withdrawn) The method of claim 37 further comprising:

planarizing said another dielectric layer to a top surface of said further conductive line; and

depositing a further layer of said another dielectric material atop said layer of said another dielectric material and atop said further conductive line.

42. (Withdrawn) The method of claim 37 said step of depositing a layer of another dielectric material includes depositing said layer of another dielectric material atop said further conductive line; and said process further comprises planarizing said another dielectric layer such that a portion thereof remains atop said further conductive line and serves as an inter-level dielectric layer.

43. (Withdrawn) A method of fabricating a semiconductor device comprising:

forming a planar gate oxide layer atop a surface of a semiconductor substrate;



PAGE 16/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

depositing at least one conducting layer atop said gate oxide layer;

patterning and etching said at least one conducting layer to form at least two openings therein;

introducing dopants into said substrate through said openings in said at least one conducting layer to form at least one source region and at least one drain region;

depositing a layer of a first dielectric material atop said surface of said semiconductor substrate;

planarizing said first dielectric layer to said top surface of said conducting layer;

depositing a layer of a further dielectric material atop said first dielectric layer and atop said conducting layer;

patterning and etching said further dielectric layer and said first dielectric layer to form at least one opening therein that includes at least one region that extends down to said source and drain regions;

depositing a contact barrier layer at least at a bottom of said opening;

annealing said contact barrier layer;

filling said opening with at least one further conducting layer;

removing at least an upper portion of said further dielectric layer to form at least one opening adjacent to said further conducting layer; and

depositing a layer of another dielectric material at least in said opening adjacent to said further conductive layer, said another dielectric material having a lower dielectric constant than that of said further dielectric material.



PAGE 17/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

44. (Withdrawn) The method of claim 43 wherein said annealing step is carried out at a temperature greater than a maximum withstand temperature of said another dielectric material.

45. (Withdrawn) The method of claim 43 further comprising: depositing an etch stop layer atop said first dielectric layer prior to depositing said layer of a further dielectric material; and wherein said step of removing at least an upper portion of said further dielectric material includes etching down to said etch stop layer.

46. (Withdrawn) The method of claim 43 wherein said step of removing at least an upper portion of said further dielectric material includes a timed etching step.

47. (Withdrawn) The method of claim 43 further comprising:

planarizing said another dielectric layer to a top surface of said further conductive layer; and

depositing a further layer of said another dielectric material atop said layer of said another dielectric material and atop said further conducting layer.

48. (Withdrawn) The method of claim 43 wherein said step of depositing a layer of another dielectric material includes depositing said layer of another dielectric material atop said further conducting layer; and said process further comprises planarizing said another dielectric layer such that a portion thereof remains atop said further conducting layer and serves as an inter-level dielectric layer.



PAGE 18/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

49. (Withdrawn) A semiconductor device comprising:

at least one deep trench formed within a semiconductor substrate;

a buried plate formed within a region of said semiconductor substrate and adjoining a bottom of said deep trench;

an insulator film formed along a lower portion of sidewalls of said deep trench;

doped polysilicon partly filling said deep trench and extending above said insulator film;

a buried strap region disposed along at least one side of said deep trench and adjoining said doped polysilicon;

a trench top oxide layer disposed atop said doped polysilicon;

a gate insulator layer formed on at least said upper portion of said side of said deep trench;

a further polysilicon layer disposed atop said trench top oxide layer and filling said deep trench with;

at least one isolation trench formed in said semiconductor substrate and adjoining said deep trench;

said isolation trench being filled with an insulator material;

a doped region formed in a top surface of said semiconductor substrate adjacent to said gate insulator layer of said deep trench;

a first conductive line disposed atop and connecting to said further polysilicon layer, said first conductive line being formed of at least one conducting layer;

a first dielectric layer extending from said surface of said semiconductor substrate to said top surface of said first conductive line;



PAGE 19/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

a further dielectric layer disposed atop said first dielectric layer and atop said first conductive line and having at least one opening therein that includes at least one region that extends down to said doped region adjacent to said gate dielectric;

an annealed contact barrier layer formed at least at a bottom of said opening; and

at least one conducting material filling a reminder of said opening to form at least one further conductive line;

at least an upper portion of said further dielectric layer being a material having a lower dielectric constant than that of a remaining portion of said further dielectric layer and having maximum withstand temperature lower than a temperature at which said contact barrier layer is annealed.

50. (Withdrawn) The semiconductor device of claim 49 wherein said upper portion of said further dielectric layer is disposed atop said further conductive line and serves as an inter-level dielectric layer.

51. (Withdrawn) A semiconductor device comprising:

a planar gate oxide layer disposed atop a surface of a semiconductor substrate;

at least one conducting layer formed atop said gate oxide layer and having at least two openings therein;

at least one source region and at least one drain region disposed in said substrate beneath said openings in said at least one conducting layer;

a first dielectric layer extending from said surface of said semiconductor substrate to said top surface of said at least one conducting layer;



PAGE 20/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

a further dielectric layer disposed atop said first dielectric layer and atop said at least one conducting layer and having at least one opening therein that includes at least one region that extends down to at least one of said source region and said drain region;

an annealed contact barrier layer formed at least at a bottom of said opening; and

at least one further conducting layer filling a reminder of said opening;

at least an upper portion of said further dielectric layer being a material having a lower dielectric constant than that of a remaining portion of said further dielectric layer and having maximum withstand temperature lower than a temperature at which said contact barrier layer is annealed.

52. (Withdrawn) The semiconductor device of claim 51 wherein said upper portion of said further dielectric layer is disposed atop said further conducting layer and serves as an inter-level dielectric layer.

53. (New) A method of incorporating first dielectric material into an insulator structure that is adjacent to at least one conductive line of a semiconductor device, said insulator structure and said at least one conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said insulator structure and said at least one conductive line at least through the thermal processing step using a second dielectric material that has a maximum withstand temperature greater than the temperature of the thermal processing step, said second dielectric material formed atop an etch stop layer;



PAGE 21/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

removing at least a portion of said second dielectric material down to said etch stop layer; and

depositing a layer of said first dielectric material in place of the removed portion of said second dielectric material.

54. (New) The method of claim 53 wherein said first dielectric material has a lower dielectric constant than said second dielectric material.

55. (New) The method of claim 53 wherein said step of fabricating said insulator structure and said conductive line includes: depositing a contact barrier layer prior to depositing said conductive line, and annealing said contact barrier layer at a temperature greater than said maximum withstand temperature of said first dielectric material.

56. (New) The method of claim 53 further comprising:

planarizing said layer of said first dielectric material to a top surface of said conductive line; and

depositing another layer of said first dielectric material atop said layer of said first dielectric material and atop said conductive line.

57. (New) The method of claim 53 wherein said step of depositing a layer of said first dielectric material includes depositing said layer atop said conductive line; and planarizing said layer of said first dielectric material such that a portion thereof remains atop said conductive line and serves as an inter-level dielectric layer.



PAGE 22/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

58. (New) A method of incorporating first dielectric material into an insulator structure that is adjacent at least one conductive line of a semiconductor device, said insulator structure and said at least one conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said insulator structure and said at least one conductive line at least through the thermal processing step using a second dielectric material that has a maximum withstand temperature greater than the temperature of the thermal processing step, said fabricating step comprising depositing a contact barrier layer prior to forming said at least one conductive line, and annealing said contact barrier layer at a temperature greater than said maximum withstand temperature of said first dielectric material;

removing at least a portion of said second dielectric material; and

depositing a layer of said first dielectric material in place of the removed portion of said dielectric material.

59. (New) A method of incorporating first dielectric material into an insulator structure that is adjacent to at least one conductive line of a semiconductor device, said insulator structure and said at least one conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said insulator structure and said at least one conductive line at least through the thermal processing step using a second dielectric material that has a maximum withstand



PAGE 23/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

temperature greater than the temperature of the thermal processing step;

removing at least a portion of said second dielectric material;

depositing a layer of said first dielectric material in place of the removed portion of said second dielectric material;

planarizing said layer of said first dielectric material to a top surface of said conductive line; and

depositing another layer of said first dielectric material atop said layer of said first dielectric material and atop said conductive line.

60. (New) A method of incorporating a first dielectric material into a semiconductor device, said semiconductor device being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said semiconductor device at least through the thermal processing step using a second dielectric material having a maximum withstand temperature greater than the temperature of the thermal processing step, said second dielectric material formed atop an etch stop layer;

removing at least a portion of second dielectric material down to said etch stop layer; and

depositing a layer of said first dielectric material in place of the removed portion of said second dielectric material.

61. (New) The method of claim 60 wherein first diclectric material has a lower dielectric constant than said further dielectric material.



PAGE 24/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

62. (New) The method of claim 53 wherein said at least one conductive line includes a contact barrier layer, and the thermal processing step is an anneal step of said contact barrier layer.

63. (New) A method of incorporating a first dielectric material into a layer of an electronic structure that includes to at least one conductive line of a semiconductor device, said layer of electronic structure and said at least one conductive line being fabricated by a process that includes at least one thermal processing step at a temperature greater than a maximum withstand temperature of said first dielectric material, said method comprising:

fabricating said layer of electronic structure and said at least one conductive line at least through the thermal processing step, said layer comprising a second dielectric material lying adjacent said at least one conductive line and said second dielectric material having a maximum withstand temperature greater than the temperature of the thermal processing step;

removing at least a portion of said second dielectric material from said layer; and

depositing a layer of said first dielectric material in place of the removed portion of said second dielectric material.

64. (New) The method of claim 63 wherein said first dielectric material has a lower dielectric constant than said second dielectric material.

65. (New) The method of claim 63 wherein said step of fabricating said insulator structure and said conductive line includes: depositing a contact barrier layer prior to depositing said



PAGE 25/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

conductive line, and annealing said contact barrier layer at a temperature greater than said maximum withstand temperature of said first dielectric material.

66. (New) The method of claim 63 wherein said step of removing at least a portion of said second dielectric material includes a timed etching step.

67. (New) The method of claim 63 further comprising:

planarizing said layer of said first dielectric material to a top surface of said conductive line; and

depositing another layer of said first dielectric material atop said layer of said first dielectric material and atop said conductive line.

68. (New) The method of claim 63 wherein said step of depositing a layer of said first dielectric material includes depositing said layer atop said conductive line; and planarizing said layer of said first dielectric material such that a portion thereof remains atop said conductive line and serves as an inter-level dielectric layer.



PAGE 26/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

## REMARKS

Claims 1, 2, 4, 7-9, 11-16, and 53-68 are pending in this application. Claims 3, 5, 6, and 10 are canceled and claims 17-52 have been withdrawn from consideration herein. Claims 1, 2, 4, 7-9, and 11-16 have been amended and claims 53-68 have been added herein. In view of these amendments and remarks, Applicant respectfully requests reconsideration of the claims.

The drawings were objected to for an improper FIG. designation. The drawings have been corrected. Replacement drawings are included herewith.

Claims 1-3, 5-7, 9-11, and 13-15 were objected to because of informalities. However, these claims have been amended such that this rejection is now moot.

In addition, claims 5, 10, and 13 were objected to as being dependent on a rejected claim. However, as discussed in detail below, the subject matter of claims 5, 10, 12, 13, and 15 is now provided in independent format. It is also noted that claims 12 and 15 were not rejected, nor were they allowed or indicated as allowable. They were, however, objected to. Therefore, applicant has treated them the same as claims 5, 10, and 13, that is, allowable if in independent form.

Claims 1-4, 6-9, 11, 14, and 16 were rejected over U.S. Patent Application No. 2002/0102843 to Seta, *et al* under 35 U.S.C. 102(b) as being anticipated, or under 35 U.S.C. 103(a) as being obvious.

More specifically, dependent claim 5 (indicated as allowable if rewritten in independent form) has been canceled and its limitations and the limitation of intervening claim 3 included in independent claim 1. Therefore, claim 1 is now allowable. Dependent claims 4, 7, and 8 have all been amended such that they depend from claim 1, as does claim 2. Therefore, claims 2, 4, 7,


PAGE 27/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

and 8 are also allowable not only for their own limitations, but also for depending from a claim deemed allowable.

Similarly, dependent claim 10 (indicated allowable) has been canceled and its limitations included in independent claim 9. Therefore, claim 9 is allowable. Dependent claims 11-16 all depend from independent claim 9 and are therefore also allowable.

Objected to (and indicated allowable) claim 13 has also been canceled and its limitations included in new independent claim 53. In addition, new claims 54-57 all depend from allowable claim 53 and are therefore believed allowable not only for their own limitations, but also for depending from a claim deemed allowable.

As mentioned above, dependent claims 12 and 15 were not rejected, but were objected to (presumably for informalities). They were not, however, objected to for being dependent on rejected parent claim 9. However, as dependent claims, these claims have also been canceled and rewritten as new independent claims 58 and 58 respectively and are believed to be allowable.

New independent claim 60 is substantially the same as amended claim 1, and includes the limitations of allowed claim 5, concerning an etch stop layer but does not include the limitations of intervening claim 3. However, it is believed that this new claim 60 is clearly patentable over the Seta, *et al.* reference, as Seta, *et al.* does not include the etch stop layer. Further, new dependent claims 61 and 62 are also believed allowable, not only for their own limitations, but also for depending from a claim deemed allowable.

New independent claim 63 has some similarity as the original claim 9, except it does not include the objected to language of the original claim 9. Further, new independent claim 63 clarifies that both the "at least one conductive line" and the dielectric material lie in the same layer unlike the Seta, *et al.* reference, wherein the low-k or first dielectric lies above the



PAGE 28/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20

conductive lines. New dependent claims 64-66 all depend from new independent claim 63 and are also believed allowable.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and requests that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge the appropriate fees to Deposit Account No. 50-1065.

Respectfully submitted,

2 August 2005
Date

James C. Kesterson
Attorney for Applicant
Reg. No. 25,882

Slater & Matsil, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, Texas 75252-5793
Tel. 972-732-1001
Fax: 972-732-9218



PAGE 29/29 * RCVD AT 8/2/2005 4:22:30 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:9727329218 * DURATION (mm-ss):06-20